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Stylesheet Version v1.1.1

Description

METHOD OF MANUFACTURE OF RAISED SOURCE DRAIN MOSFET WITH TOP NOTCHED GATE STRUCTURE FILLED WITH DIELECTRIC PLUG IN AND DEVICE MANUFACTURED THEREBY

BACKGROUND OF INVENTION

[0001] This invention relates to methods of manufacture of FET semiconductor device, and more particularly to methods of manufacture of SOI CMOS structures and devices manufactured thereby.

[0002] Scaling (reduction in dimensions) of Silicon-On-Insulator (SOI) Complementary Metal Oxide Semiconductor (CMOS) structures requires scaling of the silicon thickness to achieve device performance targets (short channel control, etc.).

[0003] FIG. 1A shows the typical structure of a prior art SOI device 10 prior to epitaxial growth of the raised source/

drain regions 28S/28D of FIG. 1B on the surface of the thin silicon layer 12 of the device 10. The device 10 includes a thin silicon layer 12 formed on a Buried OXide (BOX) layer 12. A gate electrode stack formed of dielectric (gate oxide) layer 14 upon is formed above the thin silicon layer 14, a gate electrode 18 composed of polysilicon formed above the gate dielectric layer 14, and a hard mask 22 above the gate electrode 18 has been formed. Sidewall spacers 16 composed of silicon oxide have been formed on the sidewalls of the gate electrode 18 and are intended to cover the sidewall surfaces of the of the gate electrode 18 entirely.

[0004] Note the pull-down of the spacers 16 below the hard mask 22 resulting in exposure of some of the sidewall surfaces of the polysilicon at the top corners of the gate electrode 18. This is typical of the spacer pull-down due to normal processing (spacer overetch, etc.). Reduction of this pull-down by means known heretofore would tend to reduce the robustness of the overall process (residual nitride, etc).

[0005] FIG. 1B shows the device 10 of FIG. 1A after growth of the raised source 28S and the raised drain 28D on the surface of the thin silicon layer 12. The problem which is illus-

trated by FIG.1B is that the exposure of the upper corners of the gate electrode 18 has led to spurious growth of silicon nodules 28T is seen in the region exposed at the top corners of the gate electrode 18.

[0006] The process requirement in the past has been to protect the polysilicon of the gate polysilicon 18 with spacers 16 for the purpose of avoiding the formation of spurious epitaxial growth during the raised source drain formation.

[0007] Silicidation is the process of converting a Silicon (Si) material to a silicide material. As a result of the silicidation process, the consumption of silicon thereby depends on the type of silicide being formed. For example, formation of cobalt silicide (CoSi) consumes more silicon than formation of nickel silicide (NiSi). Raised source and drain structures are required in SOI CMOS because the silicon layer in which the device is formed is reduced in thickness. This is the primary enabling element, i.e. strategy, for achieving continued reduction in silicon thickness.

[0008] The process of formation of raised source/drain regions suffers from a very limited process window. Any exposure of the gate polysilicon through either the hard mask 22 and/or above the sidewall spacers 16 results in unwanted epitaxial growth of silicon nodules 28T on the upper sur-

faces of the gate electrode 18 where they are exposed.

Summary of Invention

[0009] An object of this invention is to provide a method/process for forming a structure which eliminates the propensity for exposure of gate polysilicon.

[0010] Another object of this invention is to provide such a structure.

[0011] In accordance with this invention, a method is provided for forming an SOI MOSFET device with a silicon layer formed on a dielectric layer with a gate electrode stack, with sidewall spacers on sidewalls of the gate electrode stack and raised source/drain regions formed on the surface of the silicon layer. The gate electrode stack comprises a gate electrode formed of polysilicon above a gate dielectric layer, which is formed on the surface of the silicon layer. A cap comprising an amorphous silicon layer is formed on the top surface of the gate polysilicon. A notch is formed in the periphery of the cap layer. The notch is filled with a plug composed of a dielectric material. The plug formed in the notch extends down below the level of the top of the sidewall spacers for the purpose of eliminating the exposure of the gate polysilicon so that formation of spurious epitaxial growth during the formation of

raised source/drain regions is avoided.

Brief Description of Drawings

[0012] The foregoing and other aspects and advantages of this invention are explained and described below with reference to the accompanying drawings, in which:

[0013] FIG. 1A shows the typical structure of a prior art SOI CMOS FET device before formation of raised source/drain regions of FIG. 1B on the surface of the thin silicon layer of the device.

[0014] FIG. 1B shows the device 10 of FIG. 1A after growth of the raised source and the raised drain by epitaxial growth of silicon on the surface of the thin silicon layer with spurious growth of unwanted nodules at the upper corners of the gate electrode formed during the process of epitaxial growth.

[0015] FIG. 2A shows the device of FIG. 1A, which has been modified in accordance with this invention by forming an amorphous silicon layer on the upper surface of the gate electrode prior to forming the hard mask on the top surface of the gate electrode, above the amorphous silicon layer.

[0016] FIG. 2B shows the device of FIG. 2A after raised source/drain formation with the improvement that the epitaxial

growth is on the source and drain only without formation of any nodules of epitaxial silicon on the top corners of the gate polysilicon..

[0017] FIGS. 3A-3J illustrate the process flow in accordance with this invention for constructing the device of FIGS. 2A and 2B.

[0018] FIG. 4 is a process flow chart of the etching steps used as illustrated by FIGS. 3E to 3G to selectively undercut the selectively amorphized layer at the top of the blanket polysilicon layer and then to etch the gate polysilicon and gate dielectric to form the gate electrode.

DETAILED DESCRIPTION

[0019] Referring to FIGS. 2A and 2B, this invention provides a method for defining a raised source region 28S and a raised drain region 28D self-aligned with the gate electrode 18 and its sidewall spacers with a good process window. In particular, this invention provides a method/process for forming the structure of FIG. 1B without the growth of the spurious nodules 28T by protecting against the exposure of the polysilicon of the sidewalls of the gate electrode 18 to the epitaxial deposition process, which forms the raised source/drain regions 28S/28D.

[0020] The process requirement of the method of this invention

is to insert an additional layer of dielectric material between the gate polysilicon 18 and the spacers 26S for the purpose of eliminating the exposed polysilicon of the gate polysilicon 18 and avoiding the formation of spurious epitaxial growth during the formation of raised source/drain regions 28S/28D.

[0021] FIG. 2A shows the device 10 of FIG. 1A, which has been modified in accordance with this invention by forming an amorphous silicon layer 21B on the upper surface of the gate electrode 18 prior to forming the hard mask 22 on the top surface of the gate electrode 18, above the amorphous silicon layer. Then notches 24 (shown in FIGS. 3F and 3G) were formed at the top of the gate electrode 18 by etching away the outer edges of the amorphous silicon layer 21B. The notches 24 at the top of the gate electrode 18 were filled with dielectric plugs 26P thereby forming a Top Notched Gate (TNG) structure. The notches 24 were filled with the dielectric plug 26P to prevent formation of the kinds of nodules 28T seen in FIG. 1B on the polysilicon at the upper end of the gate electrode 18.

[0022] FIGS. 2A and 2B are analogous to FIGS. 1A and 1B, showing the structure before and after the formation epitaxial raised source/drain regions 28S/28D.

[0023] FIG. 2A shows spacer pull down to the same level as FIG. 1A, but the dielectric plug 26P prevents exposure of the polysilicon of the gate electrode 18 during the step of forming the raised source/drain regions 28S/28D.

[0024] FIG. 2B shows the device 10 of FIG. 2A after formation of the raised source/drain regions 28S/28D with the improvement that the epitaxial growth is only at the site of the source region 28S and drain regions 28D. There is no spurious growth on the top corner of the polysilicon of the gate electrode 18 of the kind seen in FIG. 1B.

[0025] FIGS. 3A-3J illustrate the process flow to construct the structure of FIGS. 2A and 2B. One advantage of this method/structure of this invention is that there is very little processing required above the normal process flow. The key is to form a top notched gate structure (TNG) with notches 24 which can then be filled with a set of dielectric plugs 26P during the normal process flow. The structure is formed using the following steps.

[0026] Preparation for the selective undercut of a thin region at the top of the gate polysilicon must be done in a controlled and repeatable manner by forming an amorphous layer on the surface of the polysilicon layer which is to be formed into a gate electrode.

[0027] FIG. 3A shows a potential gate electrode stack comprising SOI material Buried OXide (BOX) layer 11 of silicon dioxide covered with a conventional SOI thin silicon layer 12. A blanket layer of gate oxide layer 14B and a blanket polysilicon layer 18B have been formed over the BOX layer 11. The polysilicon layer 18B may be doped or undoped.

[0028] FIG. 3B shows the stack of FIG. 3A after the first step of the present invention leading to the formation of the TNG structure of this invention, which is to form a blanket, thin amorphous silicon layer 21B on the top surface of the polysilicon layer 18B in the process of ion implantation into the top surface of the blanket polysilicon layer 18 for the gate electrode 18. Germanium or silicon ions (21I) are implanted to a dose sufficient to amorphize the desired thickness of polysilicon. The thickness of the amorphous layer can be tailored by the choice of ion energy used.

[0029] FIG. 3C shows a process of gate patterning applied to the device 10 of FIG. 3B. This is done starting with the deposition over the surface of the blanket amorphous silicon layer 21B of a blanket hard mask layer 22B composed of a hard mask material (e.g. silicon nitride, TEOS, etc) and then proceeding with the initial steps of photolithographic patterning by forming a photoresist (PR) mask 23 over the

blanket hard mask layer 22B.

[0030] FIG. 3D shows the device 10 of FIG. 3C after the photoresist mask 23 has been used during etching of the hard mask layer 22B into the pattern of the photoresist mask 23, by hard mask Reactive Ion Etching (RIE) to form a hard mask 22 adapted for patterning the gate electrode stack.

[0031] FIG. 3E shows the device 10 of FIG. 3D after stripping of the PR mask 23 from the patterned hard mask 22.

[0032] FIG. 3F shows the device 10 of FIG. 3E after the TNG selective formation of the notches 24 in the amorphous silicon layer 21B of FIG. 3E as undercut notches 24 below the hard mask 22 to form amorphous silicon cap 21 between the notches 24. Selective undercut of the amorphized layer 21B to form amorphous silicon cap 21 is done during polysilicon RIE (described in detail below).

[0033] FIG. 3G shows the device of FIG. 3F, with the TNG structure after etching of the blanket polysilicon layer 18B and the blanket gate dielectric layer 14B by RIE to form the polysilicon gate electrode 18 and gate dielectric layer 14 aligned with hard mask 22. This is done with a standard RIE etch for selectively etching polysilicon with respect to the hard mask 22

[0034] FIG. 3H shows the device 10 of FIG. 3G after blanket de-

position of a spacer layer 26B composed of an appropriate spacer material covering the surface of device 10 while at the same time it is filling the notches 24 in the amorphous silicon layer 21B with material which will provide the plugs 26B seen in FIGS. 2A and 2B. The spacer material in the spacer layer 26B is composed of any spacer material such as dielectric material, e.g. silicon oxide or silicon nitride.

[0035] FIG. 3I shows the device 10 after etching back the spacer layer 26B to form spacers 26S on the sidewalls of the gate electrode 18 at the same time as plugs 26P are being formed in the undercut notches 24 at the top of the gate structure, to provide for protection of the polysilicon of the gate electrode 18 during the subsequent epitaxial raised source drain formation shown by FIG. 3J.

[0036] FIG. 3J shows the device of FIG. 3I after formation of the raised source/drain regions 28S/28D juxtaposed with the sidewall spacers 26S with no nodules formed at the top of the gate electrode 18 during the epitaxial process used to form raised source/drain regions 28S/28D.

[0037] At this point the polysilicon sidewall spacers 26S and top cap 22 can be removed and conventional process steps, as known to those skilled in the art, can be applied to fin-

ish the formation of the FET structure.

[0038] Formation of Undercut

[0039] Referring again to FIG. 3E, the etching step used to selectively undercut the selectively amorphized layer 21B at the top of the blanket polysilicon layer 18B, as well as complete the gate polysilicon etch, will now be described with reference to FIG. 4. The polysilicon etch can be adjusted to produce a precision undercut at the top of the gate layer 18B. This is accomplished by using a three step etching process. This etching process which starts at 40 in FIG. 4 is performed in a decoupled plasma etch reactor (not shown).

[0040] Formation of Top Notch/Undercut.

[0041] In step 42, the initial breakthrough and etching of the amorphized/ predoped polysilicon layer 21B is performed. This process step uses a low pressure (4-6 mT) and high bias etch (180-200W) with 80-120 HBr (hydrogen bromide) and a small amount of oxygen (O_2, 2-10 sccm). This step produces the notches 24 by undercutting the amorphous silicon layer 21B. Further, the amount of the undercut of layer 21B is very precisely controlled by the HBr/O_2 ratio.

[0042] Passivation of Top Notch/Undercut For Precision TNG Control.

[0043] In step 44, a passivation step is performed in which sidewalls of notch 24 must be passivated to maintain the notch during remainder of gate etch. This step grows a silicon oxide layer (not shown) that is thicker on the exposed surface of the implant damaged/predoped amorphous silicon layer 21B. This step uses a pressure in the range of 40-60 mT, high top source power (450-650 W) with pure oxygen (O_2, 100-150 sccm).

[0044] Horizontal Passivation Breakthrough Etch And Etching to Form the Polysilicon Gate Electrode and the Gate Dielectric Layer.

[0045] In step 46, a short breakthrough step is performed, followed by etching of the remaining polysilicon/gate dielectric stack, i.e. layers 18B/14B. The polysilicon and gate dielectric etch is a highly selectivity RIE process using materials such as HBr, Oxygen (O_2) and Helium (He) in the process. This process step uses a pressure range of 20-60 mT and top/bottom power of 200-400W and 30-100W respectively with HBr (150-300 sccm), O_2 (4-10 sccm) and He as the diluent gas. This is a standard gate polysilicon/gate dielectric etch step.

[0046] The formation of the undercut and the polysilicon/gate dielectric etching process ends at step 48, with the device 10 being removed from the decoupled plasma etch reactor.

[0047] While this invention has been described in terms of the above specific embodiment(s), those skilled in the art will recognize that the invention can be practiced with modifications within the spirit and scope of the appended claims, i.e. that changes can be made in form and detail, without departing from the spirit and scope of the invention. Accordingly all such changes come within the purview of the present invention and the invention encompasses the subject matter of the claims which follow.